SKA SIGNAL PROCESSING CONCEPT DESIGN REVIEW (SP CODR)
RESPONSE TO THE REVIEW PANEL

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LIST OF ABREVIATIONS

ADC ..... Analogue to Digital Converter
ASIC ..... Application Specific Integrated Circuit
ASKAP ..... Australian SKA Pathfinder
CoDR ..... Conceptual Design Review
DRM ..... Design Reference Mission
DSP ..... Digital Signal Processing
EVLA ..... Expanded Very Long Array
Exa ..... 10^{18}
FPGA ..... Field Programmable Gate Array
GPU ..... Graphics Processing Engine
IEAC ..... International Engineering Advisory Committee
NRE ..... Non-Recurring Expenditure
RFI ..... Radio Frequency Interference
SAB ..... System Architecture Board
SCM ..... Storage Class Memory
SEMP ..... Sytem Engineering Management Plan
SKA ..... Square Kilometre Array
SKA1 ..... SKA Phase 1
SKA2 ..... SKA Phase 2
SKADS ..... SKA Design Studies
SPDO ..... SKA Program Development Office
SPO ..... SKA Project Office
SRR ..... Sub-system Requirements Review

1 Introduction

1.1 Purpose of the document

This document provides a response to the review panel comments against the Signal Processing Concept Design Review (CoDR) for the Square Kilometre Array (SKA) project [1].

1.2 Scope of the document

This document has been written in response to the report created by the review team of the SKA Signal Processing Concept Design Review held in April 2011. The aim is to provide feedback on the comments and recommendations made.

The CoDR panel report was distributed throughout the Signal Processing community with a request to provide input to this report. Where appropriate, these have also reflected in the responses that form the main body of the document.

The structure of the response document largely follows that of the original report with responses provided against the original text including a high level summary followed by more detailed breakdown against each summary point.

2 References

[1] Robin Sharpe, Signal Processing CoDR Review Panel Review of the Review Panel WP2-040.020.011-PLA-002.

3 Response to Review Panel Summary Comments

3.1 Summary point 1

The preparation for the review was of a high standard including both the documentation, which was distributed before the meeting, and the presentations given during the review itself.

3.1.1 Response

Noted

3.2 Summary point 2

It was clear that the required signal processing concepts and algorithms were mature and in general very well understood.

3.2.1 Response

Noted

3.3 Summary point 3

Several alternative architectures are available with realisations of these utilising technologies ranging from software on a general purpose computer or graphics processing unit to FPGA and ASIC implementations.

3.3.1 Response

Noted

3.4 Summary point 4

All of the solutions presented appeared to be feasible, although estimates of cost and power consumption showed a large degree of variation.

3.4.1 Response

To some extent a variance in cost and power estimates at the CoDR is to be expected due to the low confidence associated with the basis of estimate levels particularly with respect to the SKA2 and AIP aspects of the project. However, the extent of the variation between what on the surface appear to be similar solutions is sufficiently large to require alternative explanation. A closer inspection reveals that these differences can be traced to architectural decisions and implementation efficiencies.

A simple example is the difference in implementation efficiency of the ASKAP style and Uniboard FPGA correlator concepts. The former squeezes a complex multiply per clock cycle from each FPGA DSP block compared to the latter's single multiply accumulate. This instantly creates a factor of four between the efficiencies of the two solutions. Of course, the Uniboard solution could also take advantage of this architectural trick. Future telephone conferences will encourage the sharing of implementation techniques.

3.5 Summary point 5

In moving into the next phase it will be urgent to adopt some baselines to allow proper comparisons to be made for the alternative architectures that are available.

3.5.1 Response

The importance of baselines has already been recognised at the CoDR stage with SKA Memos 125 and 130 and the DRM revision 1.3 being the datum for all concepts presented. Ultimately, the systems requirements and their flow down into the Signal Processing Element requirements will supersede these documents. The objective for the next review (the SRR) is to provide a stable and complete set of element level requirements as documented in the "Way Forward" document presented at the review.

Technology baselines were also addressed at the CoDR allowing for a further two generations of semiconductor development in terms of processing capability and power dissipation. However, it is agreed that the suggested baselines of 22nm for FPGA, GPU and x86 processor and 28nm for ASIC would form a reasonably low risk baseline for the 2015/16 time frame.

3.6 Summary point 6

The requirements for pulsar signal processing appeared to be less well developed and there was much less implementation experience evident. This area will need stronger attention in the next phase to bring it to the same level of maturity as the other areas.

3.6.1 Response

It is agreed that Non-Imaging processing requirements and concepts for the SKA are less well developed than those for correlation. This is due to the comparative complexity of its processing chain and parameter space. The requirements presented at the CoDR for pulsar signal processing and in particular Pulsar Survey largely reflects the content of the baseline documents of SKA Memo 125, 130 and the DRM revision 1.3. To address the gaps in these documents considerable work and dialogue by the contributing institutions with the Science community has been undertaken and has provided a reasonable stable but provisional set of working assumptions that are now being fed back

to the Project Scientist via the System Engineering team for consideration for a future revision of the DRM.

Although not directly applicable to summary point 6 it is worth stating that transient detection is an area that is closely coupled to Pulsar Survey but currently isn't addressed in any of the current system documentation or the phase 1 DRM. Comments received from the community in response to the Review Panel report highlight the need to provide feedback to the system engineering team to establish initial requirements for transients and whether these are at phase 1 or phase 2 of the project. However transient detection parameter space is likely to be difficult to define as it is likely to be associated with the "Detection of the Unknown" science chapter of the DRM. The response from the IEAC (International Engineering Advisory Committee) to this issue is the suggestion of the introduction of the concept of 'spigots' within the system such that third part equipment can be interfaced to the SKA system to allow flexibility in the science processing that can be achieved. The implications of spigots on the system particularly with respect to cost needs to be considered carefully including where it may be appropriate to provide the interfaces, how these interfaces might function and what additional infrastructure including space, power and cooling that would be required to support third party equipment.

The next phase will place a stronger emphasis on developing the Non-Imaging Processing in conjunction with the science and system engineering teams to provide a more stable definition of the requirements. In parallel, the contributing institutions will be encouraged to progress their experience of real time Non-Imaging Processing within the context of the SKA.

3.7 Summary point 7

Taking into account the preceding comments, the Panel believes the Signal Processing Element is ready to move into the Definition Phase.

3.7.1 Response

Noted

4 Response to Review Panel Recommendations

In its report, the CoDR panel summarized its findings in a series of 8 comments and provided 13 recommendations. The report went into further detail in separate sections on Review Preparation, Overall Impression, Preparatory Documentation, Overall Progress, Technical Adequacy and Maturity to Move into the Next Phase, Measures Identified to Address Gaps or Shortcomings, Comments related to specific questions. In the following, a response is provided to the points made by the Panel.

4.1 Recommendation 1: Architectural Level

The Project should clearly define a number of suitable architectures to be investigated further in the next phase. These will probably align with options to be carried forward into the next phase. Each of these architectures may have different impact at the system level, and these impacts should be carefully examined at both levels.

4.1.1 Response

This recommendation raises a question from the Domain Specialists perspective with respect to who has the authority to select which particular architectures are suitable for carrying forward and which

can be dropped. The SKA Founding Board work-streams are currently working towards the resolution of this ambiguity as part of the formation of the SPO office.

Another aspect of recommendation 1, that is more evident in its supporting text of the review panel report, is the need to clarify the term architecture within the context of system hierarchy illustrated in Figure 1.

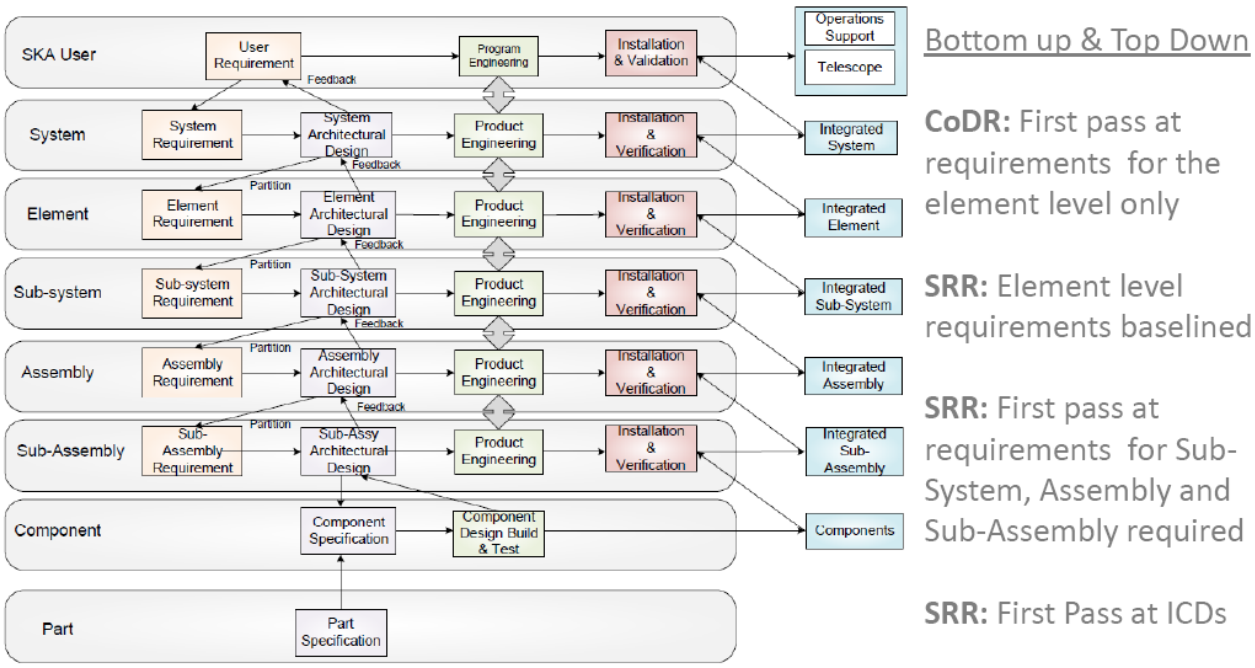

Figure 1 Hierarchy

'Architecture' is applicable across each of the layers in the system hierarchy with different connotations. The system and element levels deal primarily with functional and logical architectures and are abstracted away from the physical architecture. The CoDR only presented the FX architecture as an option for correlators. Other correlator architectures are available but the unanimous opinion across the correlator design group is that the FX architecture is the only option worth pursuing. Non Imaging processing has several architectural options identified within the high level description document. Further work is required to evaluate and quantify and document these within the next phase. It is this activity coupled with evaluation criteria (see response to recommendation 5) that will form the selection process for the most suitable element level architecture.

A similar selection process will occur at each level of the hierarchy eventually resulting in a selection process for the physical architecture. However, a top down and bottom up approach to system design has been adopted with concept implementations presented at the CoDR review. These provide a first pass at physical architectural options. It is too early to compare the individual physical architectures as many of the likely evaluation criteria such as cost have a low confidence. Consequently, all the design concepts are to be carried forward into the next phase but will be subsequently narrowed down and the impact at all levels investigated.

4.2 Recommendation 2: Measures Identified to Address Gaps or Shortcomings – Define a Fixed Element Boundary

SPDO should define a fixed boundary for the Signal Processing functions again to ensure that comparisons are meaningful, and to ensure that the participants are aware of the boundaries. If ideas for optimisation are put forward that cross the boundaries, this should be taken up at the system level.

4.2.1 Response

For the review, the aim was to have a fixed boundary of the Signal Processing defined and well documented within the High Level Description based on a hierarchical breakdown of the Signal Processing including the top level context diagram. Consequently all participants should have been fully aware of the boundaries and the working datum of SKA Memos 125 and 130 and the DRM revision 1.3.
However, some system related issues proved sufficiently compelling to some presenters that they chose to deviate from some aspects of the working datum for their concepts.
Further work within the next project phase will be implemented at the element and system levels to sell the hierarchical methodology to the contributing institutions. This is to emphasise the ability to provide feedback to the system level whilst also working to a baseline see recommendation 3.

4.3 Recommendation 3: Measures Identified to Address Gaps or Shortcomings – Optimise at the Overall System Level

The Panel recommends establishing a regularly scheduled (monthly) overall System requirements review between key Elements, where significant cross-Element optimisation could take place. This could take the form of a System Architecture Board (SAB) at the signal processing level, with a charter to be responsible for this overall optimisation. The SAB should examine or commission studies on the requirements trade-offs between various aspects of the overall SKA, where changes at that level would have a significant impact on the signal processing.

4.3.1 Response

This recommendation addresses the issues closely associated with cross domain issues such as Station Beam-forming whilst working within the well defined boundaries of recommendation 3. Consequently there is strong agreement with respect to this recommendation. It is intended that this shall be implemented using matrix style exchanges across element levels and their experts. However, it is suggested that the system engineering team will receive and ultimately ratify the resulting outcomes of these exchanges.

4.4 Recommendation 4 Measures Identified to Address Gaps or Shortcomings – Define a Common Technology Footing

Define a baseline implementation technology for the purposes of normalising performance results to allow a meaningful comparison to be made of the benefits of the alternative architectures. As an example, the Panel suggested adopting a currently available semiconductor technology generation in which CPUs, GPUs, FPGAs and ASICs are all available. Given that ASIC implementation would be one generation behind due to development delay, an approach could be to use 28nm for COTS FPGA & GPU and 40nm for ASICs. The semiconductor technology roadmap can then be used to scale all the potential solutions forwards in time on a uniform basis.

4.4.1 Response

It is agreed that defining a common technology baseline possibly constrained to the suggested limits of 28nm for COTS FPGA and GPU and 40nm for ASICs is a good idea and that the impact of Moore's Law detailed in Appendix 1 of the Review Panel Report should be taken into consideration. This will highlight the differences between communication infrastructure and firmware/software efficiency.

4.5 Recommendation 5 Measures Identified to Address Gaps or Shortcomings – Clarify and Reduce the Number of Options

There are about 200 requirements currently defined for the Signal Processing functions. The Panel felt that this was too many to handle for the selection process and recommended that the Project should define a small subset of the key requirements and evaluation criteria, perhaps 10 to 12 or so, against which the different architectural approaches can be compared. This subset should probably contain factors like cost (NRE, variable and running), power consumption, technical performance (S/N, pulsars/min.), flexibility, reliability, fault tolerance, and future proofness. The ability of an approach to exploit factors such as parallelism and locality should also be considered (see appendix I of the Review Panel Report).

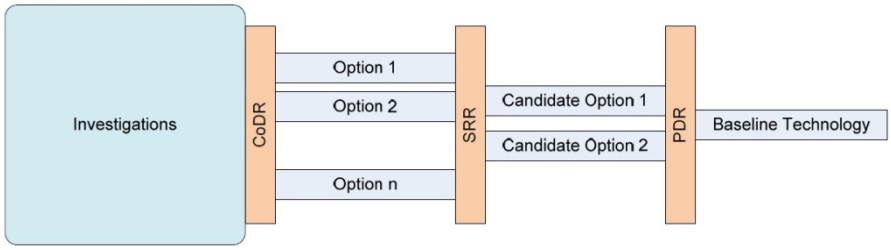

Figure 2 Narrowing down of options

4.5.1 Response

It is noted that the review panel regard the current absence of a process by which the number of options is narrowed down as an important gap. Although not yet documented, it was always intended to implement a scheme similar to that identified by the review panel i.e. a limited set of the order of 10 to 12 evaluation criteria are used in the selection process of concepts as part of the narrowing down process. The categories identified by the review panel form an excellent initial set of criteria. This can be extended by applying a weight applicable to the importance of the category of each evaluation criteria. For example, overall requirement compliance might be considered to carry a greater weight than flexibility.

It is anticipated that each concept will be scored against each category and then a weighted total generated to ascertain the most applicable concepts.

This process should not be completed until there is sufficient maturity and stability of requirements at the system and element levels and that the concepts being evaluated are traceable to the requirements. This is in line with Figure 2 taken from the SEMP where options are carried forward from the CoDR and are narrowed down at the SRR. However the evaluation criteria should be made available as soon as possible so all the development teams know what you see as critical and can aim towards achieving it.

4.6 Recommendation 6: Measures Identified to Address Gaps or Shortcomings – More Focus on Pulsar Processing

Once the pulsar search requirements, including operational requirements are clearly understood, the signal processing group should undertake an investigation of pulsar processing efficiency, using various levels of technology available ("soft" to "hard"). Assuming that acceleration searching remains a requirement, the investigation should particularly emphasise acceleration searching.

4.6.1 Response

It is noted that the review panel have identified that pulsar searching in real time and in particular acceleration processing for pulsars with relativistic binary orbits is particularly challenging. It is believed that the hard work already put in by the contributing institutions with respect to input to the high level description and the implementation concepts provide a good base for the recommended investigation of pulsar processing efficiency. This work is also being used as part of the feedback path to the system design team as in feed to the development of the pulsar search requirements.

As identified by the review panel, where more than one pulsar falls within the beam of a dish, timing can be sped up by forming several beams. Fly's eye mode has also been identified within the system requirements as a proposed mode of operation where sub-arrays may be formed to provide different pointings allowing multiple pulsars to be simultaneously timed at the expense of sensitivity. The documentation needs to be developed in association with the system engineering team.

In the supporting text in the review panel report it is suggested a cost analysis for the export of data for off-line pulsar acceleration searches as an extension of the transient detection recording system. The Technology Roadmap document provides the starting point for this analysis with cost models for hard disks as a function of time and the identification of potential future storage technology. The projected price of hard disk per Giga byte in 2015/16 (i.e. SKA1) is of the order of $0.005 and Storage Class Memory $0.1. The potential storage per 600s/ 1.25 deg2 observation for dishes presented in the High Level Description is at least 210 T Bytes which would suggest $1050 for the storage media based purely on the storage requirements. A 36,000 deg^2 all sky survey would require 6 Exa-bytes and cost at least $30M for the storage media. There will also be the cost of interface hardware and it's NRE for development and consideration for the cost of the power dissipation and cooling.

It is conceded that the omission of pulsar-synchronous operation of the imaging correlator/ spectrometer is a major hole in the documentation presented for the CoDR. This has now been fed back to the science community for consideration as in feed to the DRM with the expectation that the resultant requirements can be flowed down via the systems requirements to the Signal Processing element level. At the signal processing element level, the major implication is the provision of pulsar gating functionality within the correlator. In its simplest form correlation occurs when the gate is on, and doesn't when the gate is off. If more functionality is required, for example, having one accumulation bin when the gate is on, and one when the gate is off (or when another off-pulse gate is on), then there is an impact on correlator memory , and this can have a significant depending on the requirements and the architecture. If more than gating is implemented, i.e. pulsar phase binning where an accumulation bin for many phases of the period (say, 1000 or 2000 as in the EVLA) is required, then the impact on memory and design can be enormous.

As mentioned earlier a dialogue on this subject between the science, system engineering and Signal Processing teams is already happening with the aim of defining the requirements within the next phase.

4.7 Recommendation 7: Are the requirements complete, and sufficiently defined for this stage of the project?

Requirements should be grouped so that there is a clear delineation SKA1, SKA2 and extensibility requirements.

4.7.1 Response

The CoDR aimed to provide the first pass at the Signal Processing element level requirements and these were documented within the Requirements Document for SKA Signal Processing. This document primarily focused on Phase 1 requirements with Section 10 specifically allocated to extensibility to Phase 2 and the AIP. Consequently, it is not agreed that the document does not make a clear delineation between SKA1, SKA2 and extensibility requirements. However the requirements document is to be developed to provide a stable and largely complete set of requirements as an input to the SRR review. As part of the document development, a better context will be provided of how the requirements relate to the Systems Engineering three pronged approach detailed in Figure 1.

4.8 Recommendation 8: Are the requirements complete, and sufficiently defined for this stage of the project?

The project should acquire professional requirements management tools and use them for tracking requirements in the future. The participating organisations may also require the same tools.

4.8.1 Response

It is agreed that professional requirements management tools are required. The system engineering team are actively involved in the identification of suitable professional requirement management tools. The ability to acquire the tools at preferential cost would not appear to be a problem. However, receiving support for the tools from the vendor is also crucial and is proving to be more problematic with negotiations still ongoing.

4.9 Recommendation 9a: Are the options proposed to be carried forward credible and are the presented data and information in support of each option credible?

The SPDO should lead a process of consolidation of technical effort, where options are sufficiently similar. This should be done in conjunction with Recommendation 5 and in the light of the longer term aspect of forming work-package contractors (see the last paragraph in Section 3).

4.9.1 Response

The SPDO intends to lead a process of consolidation of technical effort based on the work-break down activities and work packages generated as part of the Project Execution Plan. This activity is currently in the process of being defined by the SKA management team and will primarily be driven by the SPO.

Interestingly, the review panel noted that some concepts appeared to be based on projection from existing pathfinder and precursor projects to the SKA. In these cases, development is likely to continue irrespective of any consolidation process.

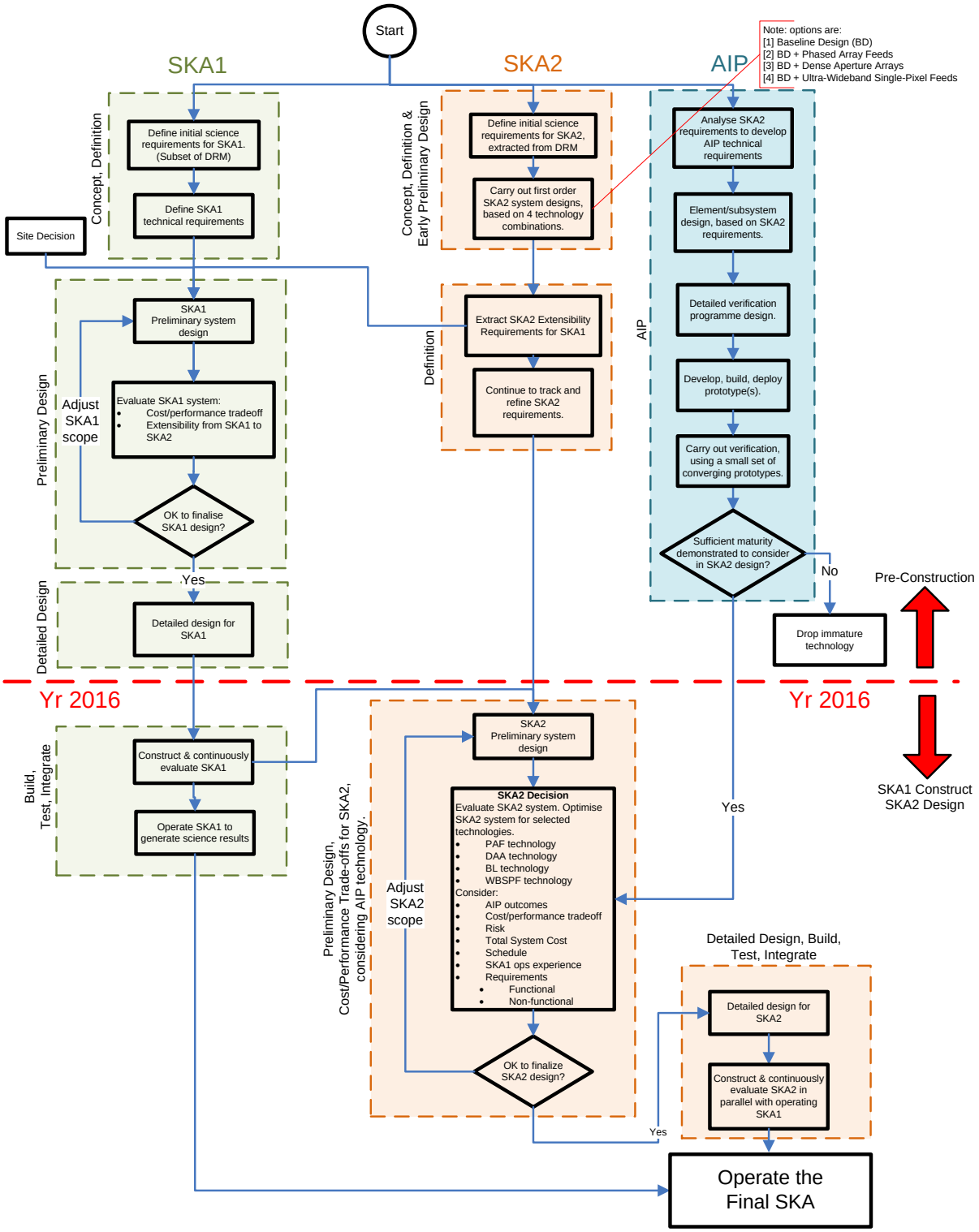

Figure 3 System Development

4.10 Recommendation 9b: Are the options proposed to be carried forward credible and are the presented data and information in support of each option credible?

There needs to be an analysis of spectral channel widths, derived from science and system-level requirements. This should lead to optimization/coordination of the spectral channelization for beam-forming with the varied time resolution requirements (and hence the bandwidth requirements) for pulsar searching and timing

4.10.1 Response

The Signal Processing high level description already contains a first pass of the detailed analysis of over-all spectral channel widths that are traceable back to system level requirements. However, aspects of the system implementation are likely to require that the over-all channelization is split. This is to include coarse channelization implemented as part of the station beam-forming and fine channelization within the signal processing. The frequency resolution required for the beam-former is a function of the array dimensions, operating frequency and RFI Mitigation. For the worst case (end fire) the AA-low phase shift beam former needs channelization to a bandwidth of much less than 1.7MHz, the central 1km core to much less than 0.3 MHz and the entire 200km phase 1 telescope 1.5kHz. Comparing these to the required time resolution of 50us for survey ~100ns for timing reveals that the processing for timing will have to include stitching frequency channels together to form the appropriate time resolution. The documentation for the SRR needs to take this into consideration. The over-all channelization scheme will be agreed across domains with co-ordination being provided by the system engineering team.

4.11 Recommendation 10: Have all the necessary aspects of the specific element/subsystem been considered and addressed during the review or are there gaps and/or shortcomings?

The signal processing group in conjunction with the system group should carry out an analysis of RFI mitigation techniques at the signal processing level, concurrently with a full inventory of RFI mitigation requirements at the system level.

4.11.1 Response

It is noted and accepted that further investigation of RFI mitigation in conjunction with the system engineering team needs to be carried out. This needs to take into account the site RFI characterisations when they become available. However, it is pointed out that the High Level Description already catalogues the RFI Mitigation strategies and their technology readiness in section 6 based on the documentation generated as part of the SKA Design Study (SKADS) programme and will be used as a starting point.

4.12 Recommendation 11: Have all the necessary aspects of the specific element/subsystem been considered and addressed during the review or are there gaps and/or shortcomings?

The signal processing group should prepare a signal path diagram beginning at the ADCs, which emphasises a signal-processing perspective in the system.

4.12.1 Response

It is agreed that an end to end signal path diagram would be a welcome addition to the Signal Processing domain documentation in providing and understanding of its context. This is best

achieved through a matrix interaction of the element level experts with respect to where trade-offs and optimisations can be made. The resultant interaction will provide input to the creation of an end to end signal path diagram which should reside at the system level. Flattening the hierarchy would prove extremely useful once a reasonable amount of stability is achieved with the over-all architecture.

It is also noted that further development of the element level block diagram within the Signal Processing High Level Description document is also needed.

4.13 Recommendation 12: Do the stated risk controls and proposed mitigations appear reasonable and executable?

The Panel agrees with the last slide in the presentation on risks, regarding actions to be taken, namely:

- Ensure that the risks currently listed are owned, managed and mitigated.
- Ensure that new risks are identified and captured.
- Continually track and monitor progress on risks.
- Review risks at the sub-system level.
- Roll up risks and inform the system risk register.

4.13.1 Response

The Signal Processing Risk Register document needs to be revised to include additional attribute columns to the risk register. These columns are to identify the risk owner and the expected retirement date of the Risk. This particular recommendation has been passed to the other element teams for inclusion in their CoDR documentation.

A dash board will be created to provide a visual indication on the progress of retiring risks. This will be created in association with the systems engineering team and will be reviewed on a regular basis.

4.14 Recommendation 13: Is the overall plan (including the identification of the tasks, effort, resources, costs, schedule and risk mitigation needed) to complete the subsequent project phases credible?

The project should ensure that the output documentation for the next phase results in a work breakdown structure that can be used subsequently in the pre-construction phase.

4.14.1 Response

The work breakdown structure is currently in the process of being defined by the SKA management team.

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